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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,869	04/07/2006	Walter Fix	411000-144	6418

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EXAMINER	
MONTALVO, EVA Y	
ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,869	FIX ET AL.	
	Examiner	Art Unit	
	Eva Montalvo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/28/2005, 02/08/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the application filed on 01/28/2006.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Kawamoto (US Patent No. 3,955,098 included in Applicant's Information Disclosure Statement and Kawamoto hereinafter).

Kawamoto discloses a device, comprising:

a circuit having an output (V_o) **and comprising at least one charging field effect transistor (charging FET)** (i.e., T_{L1}) **having source** (5), **drain** (6) **and gate electrodes** (1) **and at least one switching field effect transistor (switching FET)** (i.e., T_{D1}), **having at least one gate electrode** (7), **a source electrode** (3) **and a drain electrode** (4) (See Figs. 2A and 2B),

the drain-source electrodes of the charging and switching transistors being arranged to be coupled in series between a voltage source (V_o) **and a reference potential** (i.e., ground) **such that the gate electrode of the charging FET is not connected via an electrical line directly to the a voltage source, to the reference potential or to the output** (See Fig. 2A).

4. Claim 1-4, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Nomura (US Patent No. 6094068 and Nomura hereinafter).

5. As to claim 1, Nomura discloses a device, comprising:

a circuit having an output (2) **and comprising at least one charging field effect transistor (charging FET)** (i.e., P1) **having source, drain and gate electrodes and at least one switching field effect transistor (switching FET)** (i.e., N1)**, having at least one gate electrode, a source electrode and a drain electrode** (See Fig. 2, and col. 7 lines 59-68 and col. 8, lines 1-8)**,**

the drain-source electrodes of the charging and switching transistors being arranged to be coupled in series between a voltage source (V_{DD}) **and a reference potential** (i.e., ground) **such that the gate electrode of the charging FET is not connected via an electrical line directly to the a voltage source, to the reference potential or to the output** (See Fig. 2)**.**

6. As to claim 2, and 4, Nomura discloses a device, where:

the gate electrode of the charging FET is capacitively coupled to the source electrode of the charging FET [claim 2]**.** See Fig. 2. The examiner notes that the gate electrode of P1 is connect to the source electrode of P1 through capacitor C_{d1}.

the gate electrode of the charging FET is resistively coupled to the source electrode of the charging FET [claim 4]**.** See Fig. 2. The examiner notes that the gate electrode of P1 is connect to the source electrode of P1 through resistor R_{1a}.

7. As to claim 3, and 8, Nomura discloses a device, where:

the capacitive coupling is achieved by the gate electrode (71a) **of the charging FET** (301) **overlapping the source electrode** (21) **of the charging FET** [claim 3]**.** See Fig. 8A.

the organic logic gate is constructed without plated-though holes [claim 8]**.** See col. 7, lines 58-68 and col. 8 lines 1-33. The examiner notes that Nomura does not disclose a logic gate constructed with plated-through holes.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 5 and 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nomura in view of Bortscheller et al. (US Patent No. 4,597,001 and Bortscheller hereinafter).

Although the device disclosed by Nomura shows substantial features of the claimed invention (in paragraphs above), it fails to expressly teach:

the gate electrode of the charging FET is capacitively coupled to the drain electrode of the charging FET [claim 5]**.**

the capacitive coupling is achieved by the drain electrode overlapping the gate electrode of the charging FET [claim 6]**.**

Nonetheless, this feature is well known in the art and would have been an obvious modification of the device disclosed by Nomura, as evidenced by Bortscheller.

Bortscheller discloses a device, where:

the gate electrode of the charging FET is capacitively coupled to the drain electrode of the charging FET [claim 5]**.** See Fig. 3.

the capacitive coupling is achieved by the drain electrode overlapping the gate electrode of the charging FET [claim 6]**.** See col. 1, lines 21-26 and Fig. 3.

Given the teachings of Bortscheller, a person having ordinary skill in the art at the time of invention would have readily recognized the desirability and advantages of modifying Nomura, as suggested by Bortscheller, by overlapping the drain electrode and the gate electrode in the FET. This would ensure high transconductance between the source and drain electrode (col. 1, lines 25-26).

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nomura in view of Ker et al.(US Patent Application No. 2004/0051146 A1 and Ker hereinafter).

Although the device disclosed by Nomura shows substantial features of the claimed invention (in paragraphs above), it fails to expressly teach:

the gate electrode of the charging FET is resistively coupled to the drain electrode of the charging FET.

Nonetheless, this feature is well known in the art and would have been an obvious modification of the device disclosed by Nomura, as evidenced by Ker.

Ker discloses a device, where:

the gate electrode of the charging FET (i.e., PMOS) **is resistively coupled** (i.e., through Rp) **to the drain electrode of the charging FET**. See Fig. 3 and [0012].

Given the teachings of Ker, a person having ordinary skill in the art at the time of invention would have readily recognized the desirability and advantages of modifying Nomura, as suggested by Ker, by resistively couple the drain electrode to the gate electrode in the FET. This would allow the triggered voltage of electrostatic discharge protection of the device to be lowered to rapidly protect the thin gate oxide of the internal circuit ([0012]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Montalvo whose telephone number is (571)270-3829. The examiner can normally be reached on Monday through Thursday 7:30-5:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marcos D. Pizarro-Crespo can be reached on (571)272-1716. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eva Montalvo
Patent Examiner
Art Unit 2814
05/09/2008

/Marcos D. Pizarro/
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